IN THE SPECIFICATIONB

Page 2, second full paragraph, lines 13-16, replace the paragraph with:

The present inventor has studied data transfer control by DMAC in connection with a process such as voice codec for a GSM mobile phone, ~~of GSM~~ or the like.

Page 2, line 17 to page 3, line 2, replace the paragraph with:

For example, voice data is sampled at 8 kHz and sequentially transferred to a data processor which in turn stores the sampled data in a memory under control of DMAC. A voice compression process is executed by handling voice data of 160 samples as one lump of voice data. Since voice data is supplied even during the voice compression process, this voice data is required to be stored without deleting it under the ~~vice~~voice compression process. As a countermeasure ~~against this~~, two memory areas for storing voice data are prepared, and each time voice data of 160 samples is stored, the data transfer control conditions of DMAC are changed to thereby buffer data alternately in two memory areas.

Page 3, first full paragraph, lines 3-8, replace the paragraph with:

With this approach, however, CPU of the data processor is required to execute a process of changing the data transfer control conditions of DMAC before each voice compression process, and the process amount of CPU increases correspondingly, as the present inventor has ~~elucidated~~determined.

Page 4, line 21 to page 5, line 1, replace the paragraph with:

Even with the above-described techniques capable of continuous data transfer to a plurality of storage areas, however, a CPU load of setting the data transfer control conditions is only halved in the case of a two-area buffer. In order to further reduce the CPU load, it is necessary to increase the number of buffers. By considering limitation of resources, the above-described techniques have a limit as the present inventor has ~~elucidated~~determined.

Page 16, fourth full paragraph, lines 11-20, replace the paragraph with:

Fig. 1 shows an example of a data processor according to the invention. A data processor 1 shown in Fig. 1 has an arithmetic and logic controller 2 as a bus master

module and a direct memory access controller (DMAC) 3. The arithmetic and logic controller 2 and DMAC 3 share an address bus 4, a data bus 5 and a command bus 6. Bus privilege arbitration is performed by a bus state controller (BSC) 7 which controls the states of buses.